What is claimed is:

1. A method of performing high-speed memory testing using a low speed tester, comprising the steps of:

forming a test circuit on a memory chip on a wafer, said test circuit performing a pulse-width generator function by modifying a sync pulse on the memory chip to produce a column select signal with controlled time-on period;

forming a pulse turn-off generator on a memory chip of said wafer, said pulse turn-off generator modifying a write line signal with controlled turn-off delay;

enabling said test circuit by connecting a clock signals and a sync signal from said tester to said test circuit;

connecting a column select signal from said tester to said pulse turn-off generator of said test circuit of said memory chip, forming a column select signal with controlled time-on period;

connecting a write line from said tester to said pulse turn-off generator on a memory chip, forming a modified write line signal with controlled turn-off delay;

combining said column select signal with controlled time-on period with said modified write line signal with controlled turn-off delay, creating a write recovery period of the memory chip; and

testing said memory chip to said write recovery period.

2. The method of claim 1, wherein said test method is performed during wafer probing.

3. The method of claim 1, wherein said test method is performed during testing of a packaged memory chip using a low speed tester.

4. The method of claim 1, wherein said write recovery period is less than the period of the tester clock.

5. The method of claim 1, said pulse-width generator comprising the functions of:

receiving a clock pulse from said tester;

receiving a sync pulse from said memory chip;

passing said sync pulse from the memory chip from the input to the output of said pulse-width generator; and

delaying trailing edge of said sync pulse.

6. The method of claim 5, said delaying said trailing edge of said sync pulse being achieved in a timer circuit, which passes a leading edge quickly and delays said trailing edge.

7. The method of claim 5, said delaying said trailing edge of said sync pulse being achieved in a RC delay network of a timer

circuit, delay being adjusted by selecting a different amount of capacitance.

8. The method of claim 1, said pulse turn-off generator comprising:

receiving a row activation command;

creating a row-activation flag upon receipt of the row activation command;

initiating a column cycle;

writing a number of "n" WRPLS pulses during the column cycle;

applying the "n" WRPLS pulses as an input to a TWR reference component;

generating "n" TWR_PRO pulses by the TWR reference component;

applying the "n" TWR_PRO pulses to a capacitor which is part of the TWR reference component, the falling edges of the "n" TWR_PRO pulses charging the capacitor, the trailing edges of the "n" TWR_PRO pulses discharging the capacitor, a last falling edge of the "n" TWR_PRO pulses applied to the capacitor charging the capacitor;

internally generating a precharge command; and

ending a bit line precharge immediately after the last of said "n" TWR_PRO pulses has fallen.

9. The method of claim 8, each of said "n" TWR_PRO pulses having an adjustable pulse width in order to screen-out fail bits of the TWR specification.

10. A test circuit for performing high-speed memory testing using a slow speed tester, comprising:

forming a test circuit on a memory chip on a wafer, said test circuit performing a pulse-width generator function by modifying a sync pulse on the memory chip to produce a column select signal with controlled time-on period;

forming a pulse turn-off generator on a memory chip of said wafer, said pulse turn-off generator modifying a write line signal with controlled turn-off delay;

enabling said test circuit by connecting a clock signals and a sync signal from said tester to said test circuit;

connecting a column select signal from said tester to said pulse turn-off generator of said test circuit of said memory chip, forming a column select signal with controlled time-on period;

connecting a write line from said tester to said pulse turn-off generator on a memory chip, forming a modified write line signal with controlled turn-off delay;

combining said column select signal with controlled time-on period with said modified write line signal with controlled turn-

off delay, creating a write recovery period of the memory chip; and

testing said memory chip to said write recovery period.

11. The test circuit of claim 10, said probing said wafer being replaced by connecting said memory chip to a memory module, testing a packaged memory chip.

12. The test circuit of claim 10, said write recovery period being less than the period of the tester clock.

13. The test circuit of claim 10, said pulse-width generator comprising:

means for receiving a clock pulse from said tester;

means for receiving a sync pulse from said memory chip;

means for passing said sync pulse from the memory chip from the input to the output of said pulse-width generator; and

means for delaying trailing edge of said sync pulse.

14. The test circuit of claim 13, said means for delaying said trailing edge of said sync pulse being a timer circuit, which passes a leading edge quickly and delays said trailing edge.

15. The test circuit of claim 13, said delaying said trailing edge of said sync pulse being achieved in a RC delay network of a timer circuit, delay being adjusted by selecting a different amount of capacitance.

16. The test circuit of claim 10, said pulse turn-off generator comprising:

means for receiving a row activation command;

means for creating a row-activation flag upon receipt of the row activation command;

means for initiating a column cycle;

means for writing a number of "n" WRPLS pulses during the column cycle;

means for applying the "n" WRPLS pulses as an input to a TWR reference component;

means for generating "n" TWR_PRO pulses by the TWR reference component;

means for applying the "n" TWR_PRO pulses to a capacitor which is part of the TWR reference component, the falling edges of the "n" TWR_PRO pulses charging the capacitor, the trailing edges of the "n" TWR_PRO pulses discharging the capacitor, a last falling edge of the "n" TWR_PRO pulses applied to the capacitor charging the capacitor;

means for receiving and registering a precharge command; and

means for ending a bit line precharge immediately after the last of said "n" TWR_PRO pulses has fallen.

17. The test circuit of claim 16, each of said "n" TWR_PRO pulses having an adjustable a pulse width in order to screen-out fail bits of the Twr specification.

18. The test circuit of claim 16, pulse width variations of said "n" TWR_PRO pulses, caused by process variations in said timing reference component and the time required to write data into all cell capacitances track each other.